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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/551,266 Group Art Unit: 2816
Filing Date: September 29, 2005 Conf.: 3385
Applicant: Toshiro AKINO Examiner: O'Toole, Colleen J.
Title: LATERAL BIPOLAR CMOS INTEGRATED CIRCUIT
Attorney Docket: 9694D-000025/US

Customer Service Window October 1, 2009
Randolph Building
401 Dulany Street
Alexandria, VA 22314
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RESPONSE UNDER 37 CFR §1.116

Sir:

In response to the Examiner's Final Office Action mailed May 6, 2009, the shortened statutory period for reply having been extended by two (2) months to October 6, 2009 by a Petition for Extension of Time filed herewith, the following remarks are respectfully submitted.

Listing of the Claims begin on page 2 of this Response,

Remarks begin on page 6 of this Response.

	CLAIMS REMAINING IN RESPONSE		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA
TOTAL	8	-	20	=	0
INDEPENDENT	1	-	3	=	0